Power Efficiency in a Partially Reconfigurable Multiprocessor System

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Abstract

This poster describes the benchmarking of an FPGA-based computing system that uses partially reconfigurable tiles for real-time allocation of hardware resources. This system was developed for use in the aerospace industry in order to provide redundancy for fault mitigation and real-time hardware reallocation to reduce mass associated with separate functional systems. In this paper, we present the results of performance studies on our Xilinx Virtex-6 platform using the Dhrystone, LINPACK and NAS-Kernel benchmarks. We further present the impact on power consumption as processors and hardware accelerators are brought online to increase performance.

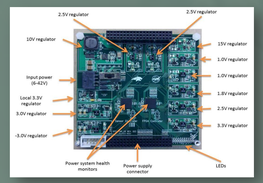
Motivation

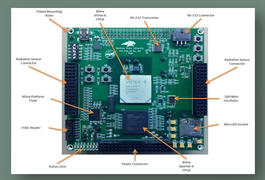
The properties of FPGAs are uniquely desirable for developing high performance computers for low power applications. The flexibility of the FPGA permits hardware designs to be specific to the end application with little hardware overhead, while the high end fabrication processes reduce power consumption. These traits are especially important in aerospace where power generation and heat dissipation are both design issues, while high computational performance is desirable.

Research Hardware

Power supply board

- Real-time power measurement
- Dynamically configurable voltage rails
- Over-current detection with auto shutdown
- Control of 12 individual voltage rails
- 6 to 42V input supply range



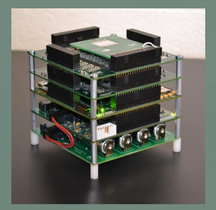


FPGA board

- Xilinx Virtex-6 and Spartan-6 devices
- Active partial reconfiguration, readback and scrubbing via 8-bit SelectMAP interface
- SD card storage, USB and RS-232 communication

Hardware Stack (1U CubeSat)

- Silicon Radiation Sensor (2x)
- FPGA Board
- Experiment board (not shown)
- Power Board
- Battery Board



System Architecture

Control FPGA

- Activates and deactivates cores on the Benchmark FPGA
- Spartan-6 75k device

Benchmark FPGA

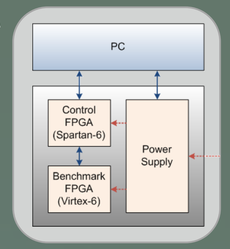
- The device being benchmarked
- Virtex-6 75k device

Power Supply

- Supplies and measures all voltages and currents in the system

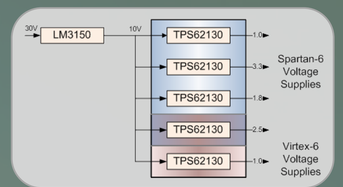
PC

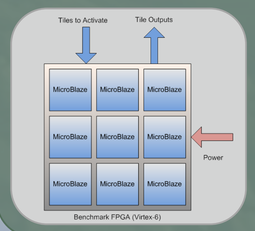
- Logs benchmark results and power consumption



Power Supply

- 12 Rails Total – Including an analog system
- 4 Voltage supplies for the Spartan-6
- 2 Voltage supplies for the Virtex-6
- Both FPGA's share the same 2.5V Rail (I/O)





Benchmark System

- 9 Tile MicroBlaze System
- Tiles can be individually activated and deactivated at runtime
- Output from tiles is output to the terminal
- Tiles are currently MicroBlaze or MicroBlaze+FPU, but agnostic in practice

Benchmarking Performance Results

Standard benchmarking routines were run on the system to establish performance and power baselines for a single core system running at 120MHz on a Virtex-6.

Dhrystone	Whetstone	LINPACK
122 DMIPS	6.3 MFLOPS (SP)	11.3 MFLOPS (SP)
		0.31 MFLOPS (DP)
		1.90 MFLOPS (DP+FPU)

A custom double floating point unit was developed for the MicroBlaze to add hardware double precision to the system. This greatly improved system performance, and is under continuing development.

The FPGA is highly flexible in the operating clock speeds. On the Virtex-6 we have successfully operated at up to 180MHz. On a per MHz basis the benchmarks were:

Dhrystone	Whetstone	LINPACK
1.01 DMIPS/MHz	52.5 KFLOPS/MHz (SP)	94.2 KFLOPS/MHz (SP)
		2.9 KFLOPS/MHz (DP)
		15.8 KFLOPS/MHz (DP+FPU)

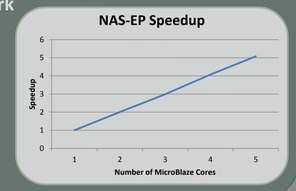
Benchmarking Performance Results (cont.)

NAS-EP Kernel (2^20 iterations):

1 Core	2 Cores	3 Cores	4 Cores	5 Cores
393 sec	195 sec	131 sec	97 sec	77 sec

- NAS benchmarks were determined to be a good fit for the system due to target applications, memory footprint, and the interconnect still being designed
- Speedup was linear as expected for this benchmark

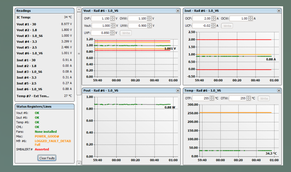
Overall speed was limited by the speed of the floating point operations, this was improved by the FPU, but additional work still needs to be completed to run the larger datasets.



Benchmarking Power Consumption

MicroBlaze power consumption was independent of the program and only affected the core power. Since the Spartan-6 could also be programmed with MicroBlaze tiles, a comparable system was built to compare the systems. The Spartan-6 had lower power consumption and quiescent currents, but also ran at a much lower speed.

Average powers were extracted, but instantaneous values are available to monitor programming power and other transient events.



Virtex-6 (120MHz) Core Powers

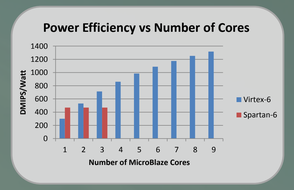
- Single Processor = 610mW
- Additional Processors = 8mW/Processor
- Double FPU = 1mW/Processor

Spartan-6 (20MHz) Core Powers

- Each processor = 130mW

Shared voltage rails:

- 1.8V = 0mW after initial programming
- 2.5V = 280mW (I/O band power)
- 3.3V = 305mW (I/O bank power)



Conclusion

The testing with the benchmarking tools to date have shown that our system is capable of running the benchmarking tools, and the monitoring capabilities of are hardware are able to record the power consumption changes in real-time as additional tiles are programmed and activated.